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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,198	02/16/2004	**Chiao-Ju Lin**	10767-US-PA	2197

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
03/25/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW
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Office Action Summary	Application No.	Applicant(s)	
	10/708,198	LIN, CHIAO-JU	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 7-16* is/are pending in the application.

4a) Of the above claim(s) *8 and 12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,9-11,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. *Claim 10* is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claim 10 recites, "*a voltage difference between the first end and the second end of the capacitor is* ***substantially equal*** *to a threshold voltage of the driving thin film transistor.*"

The original disclosure does not discuss any "***voltage difference substantially equal to a threshold voltage***" subject matter.

The Specification instead states, "*Preferably, the pre-charge voltage level is* ***close*** *to a level of the threshold voltage of the driving thin film transistor 650*" (e.g., see Paragraph 34).

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims *7 and 10* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 7 recites the limitation "***P-type***" (*in line 3*).

The addition of the word "***type***" to an otherwise definite expression extends the scope of the expression so as to render it indefinite. Ex parte Copenhaver, 109 USPQ 118 (Bd. App. 1955).

It would be unclear to one having ordinary skill in the art what "***type***" is intended to convey. See MPEP 2173.05(b).

7. The term "***substantially equal***" in claim 10 (*line 3*) is a relative term which renders the claim indefinite.

The term "***substantially equal***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

The original disclosure does not discuss any "***voltage difference substantially equal to a threshold voltage***" subject matter.

The Specification instead states, "*Preferably, the pre-charge voltage level is **close** to a level of the threshold voltage of the driving thin film transistor 650*" (e.g., see Paragraph 34).

It would be unclear to an artisan precisely how close two voltages must be before they would be considered "***substantially equal***" to one another.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. *Claims 1, 10, and 11* are rejected under 35 U.S.C. 102(b) as being anticipated by ***Yumoto (WO/2001/006484 A)***.

[*Please note: For purposes of this office action,* ***Yumoto (US 6,859,193 B1)*** *is relied upon as the English language translation of* ***Yumoto (WO/2001/006484 A)***.]

Regarding claim 1, ***Yumoto*** discloses a current-driven active matrix organic light emitting diode [*e.g., Fig. 8: AMOLED pixel*], comprising:

an organic light emitting diode [*e.g., Fig. 8: OLED*] having an anode and a cathode connected to a first power source [*e.g., Fig. 8: Vdd*];

a driving thin film transistor [*e.g., Fig. 8: TFT2b*];

a capacitor [*e.g., Fig. 8: C*] having a first end connected to a gate of the driving thin film transistor and a second end connected to a second power source [*e.g., Fig. 8: electrical ground*];

a first switch [*e.g., Fig. 8: TFT2a*] having one end connected [*via OLED*] to the anode of the OLED and another end connected [*directly*] to a drain of the driving thin film transistor;

a second switch [*e.g., Fig. 8: TFT1*] having one end connected [*via TFT3*] to a current source [*e.g., Fig. 8: CS*] and another end connected [*via electrical ground*] to the drain of the driving thin film transistor;

a third switch [*e.g., Fig. 8: TFT3*] having one end connected [*via TFT1 and electrical ground*] to the drain of the driving thin film transistor and another end connected [*via TFT4a and TFT4b*] to the gate of the driving thin film transistor and the first end of the capacitor; and

a pre-charge switch [*e.g., Fig. 8: TFT4b*] directly connected to the gate of the driving thin film transistor and a driving power source [*e.g., Fig. 8: data output from TFT4a*], wherein

the pre-charge switch controls the driving power source to pre-charge the capacitor before the current source charges or discharges the capacitor (*see the entire document, including Column 14, Lines 5-36*).

Regarding claim 10, ***Yumoto*** discloses a voltage difference between the first end and the second end of the capacitor is substantially equal to a threshold voltage [*Vth*] of the driving thin film transistor (*see the entire document, including Column 12, Line 28 - Column 13, Line 47*).

Regarding claim 11, ***Yumoto*** discloses the driving power source comprises two different voltage levels (*see the entire document, including Column 14, Lines 5-36 -- wherein TFT4a is switched on and off by scanB and TFT3 is switched on and off by scanA*).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. *Claims 7, 9, 15, and 16* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Yumoto (WO/2001/006484 A)***.

[*Please note: For purposes of this office action,* ***Yumoto (US 6,859,193 B1)*** *is relied upon as the English language translation of* ***Yumoto (WO/2001/006484 A)***.]

Regarding claim 7, ***Yumoto*** discloses the third switch being a P-type thin film transistor [*e.g., Fig. 8: TFT3*].

In the embodiment illustrated in Figure 8, ***Yumoto*** does not expressly disclose each of the first switch, the second switch, the third switch, the driving thin film transistor, and the pre-charge switch being a P-type thin film transistor.

However, in other embodiments, ***Yumoto*** discloses an N-type thin film transistor [*e.g., Fig. 26: TFT2*] being substituted with a P-type thin film transistor (*see the entire document, including Column 24, Lines 8-34*).

Therefore, it would have been obvious to one having ordinary skill in the art to replace ***Yumoto's*** N-type TFTs with P-type TFTs, so as to make a simple well known transistor substitution, and to improve the constant current properties of the circuitry, while also suppressing leakage current.

Regarding claim 9, in the embodiment illustrated in Figure 8, ***Yumoto*** does not expressly disclose the driving power source is a negative power source.

However, the embodiment illustrated in ***Yumoto's*** Figure 18 shows Vdd serving as a power source supplied to the data line (*see the entire document, including Column 20, Lines 26-36*).

Furthermore, the embodiment illustrated in Figure 26 shows Vdd serving as a negative power source (*see the entire document, including Column 24, Lines 8-37*).

Therefore, it would have been obvious to one having ordinary skill in the art to use a negative power source as ***Yumoto's*** driving power source, so as to make a simple well known power source substitution, and to improve the constant current properties of the circuitry, while also suppressing leakage current.

Regarding claim 15, ***Yumoto*** discloses the first power source is of negative polarity [*e.g., Fig. 26: negative potential Vdd*] (*see the entire document, including Column 24, Lines 8-37*).

Therefore, it would have been obvious to one having ordinary skill in the art to use a negative power source as ***Yumoto's*** first power source, so as to make a simple well known power source substitution, and to improve the constant current properties of the circuitry, while also suppressing leakage current.

Regarding claim 16, ***Yumoto*** discloses that "*any constant potential*" may serve as ground (*see the entire document, including Column 5, Lines 34-36*).

Therefore, it would have been obvious to one having ordinary skill in the art to use a positive power source as ***Yumoto's*** second power source, so as to make a simple well known power source substitution, and to improve the constant current properties of the circuitry, while also suppressing leakage current.

Response to Arguments

12. Applicant's arguments filed on *18 January 2010* have been fully considered but they are not persuasive.

The Applicant contends, "*the interpretation of the terminology 'P-Type' or 'N-type' is definite*" (see Page 7 of the Response filed on *18 January 2010*). However, the examiner respectfully disagrees.

Claim 7 includes the limitation "***P-type***" (*in line 3*). The addition of the term "***type***" to an otherwise definite expression extends the scope of the expression so as to render it indefinite. Ex parte Copenhaver, 109 USPQ 118 (Bd. App. 1955). It would be unclear to an artisan what "***type***" is meant to convey. See MPEP 2173.05(b).

The Applicant contends, "*the terminology 'substantially equal' recited in claim 10 is definite*" (see Page 7 of the Response filed on *18 January 2010*). However, the examiner respectfully disagrees.

The term "***substantially equal***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree (*e.g., the term "substantially equal" is not found anywhere within the specification*), and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

The original disclosure does not mention any "***voltage difference substantially equal to a threshold voltage***" subject matter.

The Specification instead teaches, "*Preferably, the pre-charge voltage level is **close** to a level of the threshold voltage of the driving thin film transistor 650*" (e.g., see Paragraph 34).

It would be unclear to an artisan precisely how close two voltages should be before they would be considered "***substantially equal***" to each another.

The Applicant contends, "*the TFT2a disclosed by **Yumoto** is NOT electrically connected to the drain of the TFT2b*" (see Page 8 of the Response filed on *18 January 2010*). However, the examiner respectfully disagrees.

Firstly, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "*electrical connections*") are not recited in the rejected claims.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Secondly, the Applicant acknowledges that one qualifying type of "*connection*" is an "*indirect connection, meaning... physically connected to other circuit elements first*" (*see Page 12 of the Response filed on 6 May 2008*).

The Applicant also acknowledges that one other qualifying type of "*connection*" is an "*electrical connection*" (*see Page 8 of the Response filed on 18 January 2010*).

Additionally, claim 1 recites the subject matter: "*an organic light emitting diode (OLED) having an anode and a cathode connected to a first power source*" (*see lines 3-4*).

Such a claimed "*connection*" is clearly NOT a direct physical connection -- it must instead be a "*physically indirect connection*" and/or an "*electrical connection*."

Furthermore, the Applicant explicitly distinguishes between the above "*physically indirect connections*" and "*electrical connections*" by adding one "*direct connection*" limitation to claim 1 (*see line 15*).

Therefore, it is fair to presume all the other claimed "*connections*" are not required to be "*direct connections*."

Thirdly, ***Yumoto*** does disclose a first switch [*e.g., Fig. 8: TFT2a*] having

one end [*e.g., Fig. 8: TFT2a's upper drain*] connected [*electrically / indirectly*] to the anode of an OLED [*e.g., Fig. 8: OLED*] and

another end [*e.g., Fig. 8: TFT2a's lower source*] connected [*electrically / directly*] to a drain of the driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*].

The Applicant contends, "*the Office Action interpreted that terminal 'D1' as the drain of the TFT2b. Furthermore, in Page 6 lines 1-6, the Office Action the Office Action interpreted that terminal 'D2' as the drain of the TFT2b. Obviously, the terminals 'D1' and 'D2' are simultaneously interpreted as the drain of the TFT2b. Applicant submits that the interpretation regarding to the darin of the TFT 2b is improper and the 35 U.S.C 102 rejection should be withdrawn accordingly*" (see Pages 8-9 of the Response filed on *18 January 2010*). However, the examiner respectfully disagrees.

Firstly, the "*D1*" & "*D2*" terminology is of the Applicant's own making. The examiner did not use such terminology in this or the prior Office action.

Secondly, neither this nor the prior Office action relies on multiple or contradictory interpretations of what constitutes the drain of ***Yumoto's*** TFT2b [*see Fig. 8*].

TFT2b's source (*i.e., the lower terminal*) is illustrated in Figure 8 as being directly connected to the electrical ground line.

TFT2b's drain (*i.e., the upper terminal*) is illustrated in Figure 8 as being directly connected to TFT2a's source (*i.e., the lower terminal*).

As explained earlier, ***Yumoto*** discloses a first switch [*e.g., Fig. 8: TFT2a*] having

one end [*e.g., Fig. 8: TFT2a's upper drain*] connected [*electrically / indirectly*] to the anode of an OLED [*e.g., Fig. 8: OLED*] and

another end [*e.g., Fig. 8: TFT2a's lower source*] connected [*electrically / directly*] to a drain of the driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*].

Yumoto also discloses a second switch [*e.g., Fig. 8: TFT1*] having

one end [*e.g., Fig. 8: TFT1's upper drain*] connected [*electrically / indirectly via TFT3*] to a current source [*e.g., Fig. 8: CS*] and

another end [*e.g., Fig. 8: TFT1's lower source*] connected [*electrically / indirectly via the ground line and TFT2b's lower source*] to the drain of the driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*].

Yumoto's second switch [*e.g., Fig. 8: TFT1*] is connected [*electrically / directly*] to the ground line.

The drain of ***Yumoto's*** driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*] is connected [*electrically / indirectly via TFT2b's lower source*] to the ground line.

Therefore, ***Yumoto's*** second switch [*e.g., Fig. 8: TFT1*] is indeed "*connected*" [*electrically / indirectly*] with the drain of the driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*], as presently claimed.

Yumoto then discloses a third switch [*e.g., Fig. 8: TFT3*] having

one end [*e.g., Fig. 8: TFT3's left drain*] connected [*electrically / indirectly via TFT1, the ground line, and TFT2b's lower source*] to the drain of the driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*] and

another end [*e.g., Fig. 8: TFT3's right source*] connected [*electrically / indirectly via TFT4a and TFT4b*] to the gate of the driving thin film transistor [*e.g., Fig. 8: TFT2b's gate*] and the first end of the capacitor [*e.g., Fig. 8: the top electrode of capacitor C*].

The source of ***Yumoto's*** second switch [*e.g., Fig. 8: TFT1's lower source*] is connected [*electrically / directly*] to the ground line.

Yumoto's third switch [*e.g., Fig. 8: TFT3*] is connected [*electrically / indirectly*] to the ground line through the second switch [*e.g., Fig. 8: TFT1*], when the second switch [*e.g., Fig. 8: TFT1*] is closed.

The drain of ***Yumoto's*** driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*] is connected [*electrically / indirectly via TFT2b's lower source*] to the ground line.

Therefore, ***Yumoto's*** third switch [*e.g., Fig. 8: TFT3*] is indeed "*connected*" [*electrically / indirectly via TFT1, the ground line, and TFT2b's lower source*] with the drain of the driving thin film transistor [*e.g., Fig. 8: TFT2b's upper drain*], as presently claimed.

The Applicant is respectfully reminded that every circuit element illustrated in ***Yumoto's*** Figure 8 is "*connected*" [*via at least an electrical connection or a physically indirect connection*] to all the other illustrated circuit elements:

Each transistor is "*connected*" to all the other transistors.

The OLED is "*connected*" to all the transistors.

The OLED is "*connected*" to the capacitor.

The OLED is "*connected*" to the current source.

The capacitor is "*connected*" to all the transistors.

The current source is "*connected*" to all the transistors.

The current source is "*connected*" to the capacitor.

The ground line is "*connected*" to all the transistors.

The ground line is "*connected*" to the capacitor.

The ground line is "*connected*" to the current source.

If ***Yumoto's*** pixel circuit elements were not all connected, they would not constitute a "*circuit*."

Applicant's arguments with respect to claims 7 and 10 have been considered but are moot in view of the new grounds of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
19 March 2010